

**Remarks**

Claims 10-20 are pending in the application following entry of this Amendment. Dependent Claims 16 and 17, indicated by the Office Action as containing allowable subject matter, are amended with the subject matter of independent claim 10.

Claim 10 is amended to recite, storing and updating fault injection selection data in a first register in response to a first clock signal; and scanning and storing fault injection values in a second register in response to a second clock signal independent of the first clock signal. Antecedent basis appears in paragraph [0037] at page 9, lines 13-16, and in Applicants' Fig. 1. Data corruption due to rippling is avoided, as described in paragraph [0037]. New claims 19 and 20 similarly recite the amended recitals of claim 10.

**Rejection Pursuant to 35 U.S.C. § 102(e) in view of Nadeau-Dostie, et al., U.S. 6,536,008 B1.**

In the cited reference, Nadeau-Dostie, et al., Fig. 6 differs from Applicants' Fig. 1. Figure 6 shows a *Fault-Enable* signal and a *SelectJtagOutput* signal applied to a single gate 116. Fig. 7 shows a similar single gate 148. Fig. 8 shows a similar single gate 172. Fig. 9 shows a similar single gate 194. Fig. 10 shows a similar single gate 214. Thus, the single gate of Nadeau-Dostie is controlled by a single clock signal. Claim 10 is amended to distinguish from a single gate controlled by a single clock signal, as in Nadeau-Dostie.

Further, the reference discloses, at column 7, lines 7-18, The multiplexer has two inputs 102 and 104 for receiving a pair of fault type signals, *FaultyZeroOut* and *FaultyOneOut*, respectively... *FaultyZeroOut* is set active when a stuck-at 0 fault is to be injected...*FaultyOneOut* is active when a stuck-at 1 fault is to be injected....The Update latch 62 stores the fault value. Further, at column 7, lines 53-54, "When both *FaultyZeroOut* and *FaultyOneOut* are asserted, all Boundary Scan cells will enter an external test mode."

Applicants' claim 10 is amended to recite, in part, "scanning and storing fault injection values in a second register in response to a second clock signal independent of

the first clock signal, wherein the fault injection values comprise either stuck-at fault injection values or stuck-on fault injection values." Thereby, amended Claim 10 differs from the two inputs 102 and 104 of the reference. New claims 19 and 20 similarly recite the amended recitals of claim 10.

Claims 12, 15 and 18 are grouped together with Claim 10 for purposes of patentability.

**Rejection Pursuant to 35 U.S.C. § 103(a) in view of Nadeau-Dostie, et al., U.S. 6,536,008 B1 in view of Abramovici et al., U.S. 6,202,182 B1.**

Claims 11, 13 and 14 are grouped with Claims 10, 12, 15 and 18 for purposes of patentability.

In view of the amendments and Remarks supporting patentability of the claims, allowance is requested.

The Examiner is invited to telephone the undersigned to request assistance in advancing the prosecution of the application.

Respectfully submitted,

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Enclosure: IDS and cited NPR